SIDDHARTH GROUP OF INSTITUTIONS :: PUTTUR
Siddharth Nagar, Narayanavanam Road – 517583

QUESTION BANK (DESCRIPTIVE)

Subject with Code : Digital Logic Design(16CS506) **Course & Branch**: B.Tech - CSE

Year &Sem: II-B.Tech& I-Sem

UNIT –I

Binary Systems, Boolean Alegebra

1. 1. a) Convert the following numbers (L5) (5M)

   i)$(41.6875)_{10}$ to Hexadecimal number ii)$(11001101.0101)_2$ to base-8 and base-4iii)$(4567)_{10}$ to base2

   b) Subtract $(111001)_2$ from (101011) using 1's complement? (L5) (5M)

2. a)Represent the decimal number 3452 in i)BCD ii)Excess- (L5)(3M)

   b) perform (-50)-(-10) in binary using the signed-2's complement (L5)(3M)

   c) Determine the value of base x if$(211)x=(152)_8$ (L5) (4M)

3. a)Convert the following numbers (L5) (3M)
   i) $(AB)_{16}$ = ( )$_2$ ii)) $(1234)_8$ = ( )$_{16}$ iii)$(101110.01)_2$=( )$_8$

   b) Convert the following to binary and then to gray code $(AB33)_{16}$ (L5) (3M)

   c) Perform the following Using BCD arithmetic $(7129)_{10}$ + $(7711)_{10}$ (L5) (4M)

4. Simplify the Boolean expressions to minimum number of literals (L5) (10M)
   i) **(**A + B)(A + C')(B' + C')
   ii) AB + (AC)' + AB'C(AB + C)
   iii) (A+B)' (A'+B')'
5. Explain the Binary codes with examples? (L2) (10M)
6. Explain about complements with examples? (L2) (10M)
7. a)Simplify the Boolean expressions to minimum number of literals (L5) (5M)

   i) X' + XY + X Z' + XYZ' ii) (X+Y) (X+Y')

   b) Obtain the Complement of Boolean Expression (L5) (5M)

   i) A+B+A'B'C ii) AB + A (B +C) + B'(B+D)
8. Convert the following (L5) (10M)

   a)$(1AD)_{16}$=( )$_{10}$ b) $(453)_8$=( )$_{10}$ c) $(10110011)_2$=( )$_{10}$ d) $(5436)_{10}$=( )$_{16}$

9. a) The solution to the quadratic equation x^2-11x+22=0 is x=3 and x=6 what is the base of the number (L5) (5M)

Convert the following numbers (L5) (5M)

i) $(615)_{10}$ = ( )$_{16}$ ii)) $(214)_{10}$ = ( )$_{8}$ iii)$(0.8125)_{10}$=( )$_{2}$

iv) $(658.825)_{10}$=( )$_{8}$ v)$(54)_{10}$=( )$_{2}$

10. a) Explain the Excess-3 code? (L2) (5M)

b) Write about Error correction & Detection? (L2) (5M)

UNIT –II

Gate Level Minimization

1. Simplify the following Boolean expression using K-MAP and implement using NAND gates. F(W,X,Y,Z) = XYZ+WXY+WYZ+WXZ (L5) (10M)
2. Simplify the Boolean expression using K-MAPF(A,B,C,D) = ∑m(1,2,3,8,9,10,11,14) +d(7,15) (L5) (10M)
3. Simplify the Boolean expression using K-map and implement using NAND gates

   F(A,B,C,D) = ∑m(0,2,3,8,10,11,12,14) (L5) (10M)
4. Reduce the expression f(x,y,z,w)= πM(0,2,7,8,9,10,11,15) .d (3,4) using K-Map?(L5) (10M)
5. Simplify the Boolean expression using K-map? (L5)(10M)
   F(A,B,C,D,E)= ∑m(0,1,4,5,16,17,21,25,29)
6. Obtain the minimal product of sums and design using NAND gates (L5)(10M)
   F(A,B,C,D)= = ∑m(0,2,3,6,7) +d(8,10,11,15)
7. Explain NAND- NOR implementations? (L5) (10M)
8. a) Design the circuit by Using NAND gates F= ABC'+ DE+ AB'D' (L5) (5M)

   b) Design the circuit by Using NOR gates F= (X+Y). (X'+Y'+Z') (L5) (5M)
9. Simplify the Boolean expression using K-MAP (L5) (10M)

F(A,B,C,D,E)= ∑m(0,2,4,6,9,11,13,15,17,21,25,27,29,31)

10. Simplify the Boolean expression using K-MAP (L5) (10M)

    F(A,B,C,D) = πM (3,5,6,7,11,13,14,15) .d(9,10,12)

UNIT –III

Combinational Logic

1. Explain Carry Lookahead Generator ? (L5) (10M)
2. A)Implement the following Boolean function using 8:1 multiplexer (L5) (5M)

   F(A, B, C, D) = A'BD' + ACD + A'C' D +B'CD

   B)Explain about parallel adderAdder? (L2)(5M)
3. A) Explain Design Procedure of combinational circuits? (L2) (5M)

   B) Explain Fullbinarysubtractor in detail? (L2) (5M)
4. Design the combinational circuit binary to gray code? (L5) (10M)
5. A)Explain about Binary Half Adder? (L2) (5M)

   B)What is Full Adder? Design & Explain the operations of Full Adder ? (L2) (5M)
6. A)Implement the following Boolean function using 8:1 multiplexer (L5)(5M)

   $F(A,B,C.D) = \Sigma m\ (0,1,2,5,7,8,9,14,15)$

   B) Explain about Decimal Adder? (L2) (5M)
7. A)Design a 4 bit adder-subtractor circuit and explain the operation in detail? (L5) (5M)

   B) Explain the functionality of a Multiplexer? (L2) (5M)
8. Implement BCD to 7-segment decoder for common anode using 4:16 decoder? (L5) (10M)
9. A)Design a 4 bit binary parallel subtractorand the explain operation in detail? (L5) (5M)

   B) Design the combinational circuit of Binary to Excess-3 code convertor? (L5) (5M)
10. A)What is combinational circuits and explain analysis and design procedure of combinational circuits ? (L2)(5M)

    B)Explain about Priority encoder? (L5) (5M)

UNIT –IV

Synchronous Sequential Logic

1. A) Explain the Logic diagram of JK flip-flop? (L2) (5M)

   B) Write difference between Combinational & Sequential circuits? (L4) (5M)
2. A) Explain the Logic diagram of SR flip-flop? (L2) (5M)

   B) Design and draw the 3 bit up-down synchronous counter? (L5) (5M)
3. A) Draw and explain the operation of D Flip-Flop? (L5) (5M)

   B) Explain about Shift Registers? (L2) (5M)
4. A) Draw and explain the operation of T Flip-Flop? (L5) (5M)

   B) Explain about Ring counter? (L2) (5M)
5. A) Explain about ripple counter? (L2) (5M)

B) What is state assignment? Explain with a suitable example? (L2) (5M)

6. Explain the working of the following (L2 & L5) (10M)

i) J-K flip-flop

ii) S- R flip-flop

iii) D flip-flop

7. Explain the design of a 4 bit binary counter with parallel load in detail? (L2) (10M)

8. What is race-around condition? How does it set eliminate is a Master –slave J-K flip-flop? (L2)(10M

9. A) Explain synchronous and ripple counters compare their merits and demerits? (L2) (5M)

B) Design a 4 bit binary synchronous counters with D-flip flop? (L5) (5M)

10. a)Write the truth table of clocked T- Flip Flop? (L1)(3M)

b) Write the differences between latches and flip flops? (L1)(4M)

c) Write the differences between synchronous and asynchronous counters? (L1)(3M)

UNIT –V

Memory and Programmable Logic , Digital Logic Circuits

1. A) Write difference between PROM&PLA &PAL? (L4) (5M)

B) Explain about Error correction & Detection Codes ? (L2) (5M)

2. Encode the 11-bit code 10111011101 into 15 bit information code? (L3)(10M)

3. Implement the following function using PLA (L5)(10M)

$A(x,y,z)=\sum m(1,2,4,6)$ $B(x,y,z)=\sum m(0,1,6,7)$ $C(x,y,z)=\sum m(2,6)$

4.Design PAL for a combinational circuit that squares a 3 bit number? (L5)(10M)

5. What is memory decoding? Explain about the construction of 4 X 4 RAM ? (L2) (10M)

6. Construct the PROM using the conversion from BCD code to Excess-3 code? (L5)(10M)

7. Implement the following functions using PLA. (L5)(10M)

$A(x,y,z) = \sum m(1,2,4,6)$ $B(x,y,z) = \sum m(0,1,6,7)$ $c(x,y,z) = \sum m(2,6)$

8. A)Construct the PLA using the conversion from BCD code to Excess-3 code?(L5)(10M)

9. A)Explain about Hamming Code with example? (L2)(5M)

B) Explain about memory decoding error detection and correction? (L2)(5M)

10.A)Explain different types of ROM? (L1) (5M)

B) Write a short notes on Programmable array Logic? (L1) (5M)

SIDDHARTH GROUP OF INSTITUTIONS :: PUTTUR
Siddharth Nagar, Narayanavanam Road – 517583

QUESTION BANK (OBJECTIVE)

Subject with Code : Digital Logic Design(16CS506) **Course & Branch**: B.Tech - CSE

Year &Sem: II-B.Tech& I-Sem

UNIT – I

Binary Systems, Boolean Alegebra

1. (75.23) is a Octal number convert to it equivalent binary number [ ]

   A) 1110111.110111 B)111110.010110 C)1111111.110110 D)111101.010011

2. 9's complement of 1234 is [ ]

   A) 8764 B) 8765 C) 7886 D) 7768

3. Find 2's complement of (11000100)_____ [ ]

   A) 00111100 B) 110000100 C) 1010101010 D) none

4. Non-weighted code is _____ [ ]

   A) Gray code B) Decimal C) Binary D) octal

5. Decimal value base is_____ [ ]

   A) 10 B) 8 C)16 D) 2

6. A^1B^1 =_____ [ ]

   A) A^1+B^1 B) $(A+B)^1$ C) AB D) A+B

7. Which gate have any one input is high then the output is high [ ]

   A)EX-OR B)NAND C)NOTD) EX-NOR

8. Convert 0.5 decimal number to its binary equivalent_____ [ ]

   A)0.1011 B) 0.1011 C) 0.1000 D) 0.1010110

9. BCD code for 92 [ ]

   A) 011010010010 B) 000100000101 C) 10010010 D) 10010011

10. 10's complement of $(52520)_{10\ is}$_____ [ ]

    A)42479 B)47479 C)47480 D)47481

11. $(52)_8$ is decimal equivalent to [ ]

    A) $(50)_{10}$ B) $(42)_{10}$ C) $(64)_{10}$ D) $(35)_{10}$

12. A decimal number 19 is in excess 3 code is written as [ ]

    A) 00110 B) 10110 C) 10110 D) 0011

13. The higher significant bit of this result is called_____ [ ]

    A) Sum B) carry C) 0 D) none

14. Distributive law is_____ [ ]

    A) A(B+C) =AB+AC B) AB=BA C) A+(B+C)=(A+B)+C D) none

15. A+1 =_____ [ ]

    A) A B) 1 C) 0 D) none

16. ABC+ABC'=_____ [ ]

    A) A B) AB C) C D) AC

17. A+AB=_____ [ ]

    A) 1 B)0 C) A D) none

18. Decimal 20 is in binary number system is [ ]

A) 10101 B) 1111 C) 10100 D) 11001

19. Find 1's complement of (11010100)_____ [ ]

A) 00101011 B) 11010100 C) 101010100 D) none

20. What is the maximum number of different boolean functions involving n Boolean variables? [ ]

A) n^2 B)2^n C)2*n D)2^{2n}

21. _____ bit represent the sign of the number [ ]

A) MSB B)LSB C)both D)none

22. Which gate is generate complement of output to given input _____ [ ]

A) NOT B) NAND C)OR D) XNOR

23. _____ codes are non weighted codes [ ]

A) Gray B) decimal codes C) binary D) none

24. (A+B)+C=A+(B+C) is _____ law [ ]

A) Associative law B) commutative law C) Distributive law D) none

25. Example of weighted code_____ [ ]

A) gray B) 8421 C) excess-3 D) none

26 . 111001 is a binary value convert to it equivalent octal_____ [ ]

A) 71 B) 70 C) 15 D) 11

27. 27 is a octal value convert to it equivalent decimal_____ [ ]

A) 8 B) 23 C) 33 D) none

28. ASCII stand for_____ [ ]

A)American standard coded for information interchange

B) American standard coded for interchange information C) both D) none

29. _____ theorem states that A+B= B+A [ ]

A)Consensus theorem B) duality C) associative law D) commutative

30. $A.A^1$=_____ [ ]

A)1 B)0 C) A D) none

31. $A+A^1B$=_____ [ ]

A) A+B B) A+BA C) 0 D) none

32. Convert AB6 to binary [ ]

A) 101011010010 B) 101010110110 C) 10101010101 D) 10101111

33. Product terms is also called as_____[ ] A) Max terms B) MintermsC)both A&B D) none

34. (r-1)'s complement is also called as [ ]

A)Radix B) Dimnished radix C)2 D)15

35. Which gate is generate complement of output to given input _____ [ ]

A) NOT B) NAND C)OR D) XNOR

36. The _____ of digital logic gate refers to the number of inputs [ ]

A) Fan-in B) fan-out C) both D) none

37. Sum terms is also called as_____ [ ]

A) Max terms B) Minterms C)both A&B D) none

38. (A+B)+C=A+(B+C) is _____ law [ ]

A)Associative law B) commutative law C) Distributive law D) none

39. $(231)_4$convert to decimal value [ ]

A) 45 B) 43 C) 42 D) none

40. 53 is decimal value convert to its binary value [ ]

A) 110101 B) 110010 C) 110101 D) 11001

UNIT – II

Gate Level Minimization

1. Vietch diagram also known as _____ [ ]

A) Karnaugh map B) logic gate C) BSD D) none

2. 2 variable k map contains _____ cells [ ]

A)8 B) 4 C)2 D)12

3. The map method is first proposed by_____ [ ]

A) Vietch B) charlas C) karnaughD) none

4. A grouping of 8 bits in K-map known as_____ [ ]
   A)byte B) octet C) quad D) isolated
5. Example of UNIVERSAL GATE is_____ [ ]
   A)NAND B)NOT C) OR D) none
6. The code used for labeling the cells of k map is_____ [ ]
   A) gray B) octal C) BCD D) none
7. AND Gate requires_____ Minimum number of inputs. [ ]
   A)2 B)1 C)4 D) none
8. A pair is a group of _____ adjacent cells in a k-map [ ]
   A) 2 B) 4 C)8 D) 16
9. 3 variable k map contains _____ cells [ ]
   A) 6 B) 8 C) 5 D) 3
10. _____ is a group of 8 adjacent cells in K-Map [ ]
    A)octet B)pair C) quad D) none
11. don't care condition represented label as_____ [ ]
    A) S B) X C) d D)both B&C
12. The output levels are indicated by "X" or "d" in the truth tables and are called __ [ ]
    A) don't care conditions B) minterms C) output D) none
13. Which gate is not universal gate_____ [ ]
    A) NAND B) NOR C) XOR D) none
14. Consider the following Boolean function of four variables f(w,x,y,z)=∑m(1,3,4,11,12,14) The function is [ ]
    A)independent of one variable B)independent of two variables
    C) independent of three variables D) Dependant on all the variables

15. 4 variable k map contains _____ cells [ ]
    A) 12 B) 16 C) 15 D) 3
16. In K-map Pair eliminates _____variable from output expression. [ ]
    A) One B)Two C)Three D)Zero
17. In K-map Quad eliminates _____variable from output expression. [ ]
    A) One B)Two C)Three D)Zero
18. In K-map octet eliminates _____variable from output expression. [ ]

A) One B)Two C)Three D)Zero

19. 5 variable k map contains _____ cells [ ]

A) 32 B) 36 C) 15 D) 3

20. The sum of all the minterms of a given Boolean function is equal to [ ]

A) Zero B)One C)Two D)Three

21. The product of all the maxterms of a given Boolean function is equal to [ ]

A) Zero B)One C)Two D)Three

22. Let f(A,B) = A+B, simplified expression for function f(f(x+y,y),z) is [ ]

A)x+y+z B)xyz C)1 D)xy+z

23. Maximum number of prime implicants with n binary variable in the reduced expression is [ ]

A) 2^n B) 2*n C)2^{n-1} D)2+n

24.The Logical expression y=∑m(0,3,6,7,10,12,15) is equivalent to [ ]

A) Y= πM(0,3,6,7,10 ,12,15) B)y= πM(1,2,4.,5,8,9,11,13,14)

C) Y= ∑M(0,3,6,7,10 ,12,15) B)y= ∑M(1,2,4.,5,8,9,11,13,14)

25. The minimum number of 2 input NAND gates required to implement the following Boolean function f= (x'+y')(z+w) [ ]

A) 3 B)4 C)5 D)6

26.What is the value of B+B'A [ ]

A)A B)B C)0 D)A+B

27._____ method is used for to simplify the boolean expressions [ ]

A) K-map B)Algebric rules C)Tabular method D)ALL

28. The pictorial representation of truth table is also called as____ [ ]

A) K-Map B)Tabular map C)Both A&B D)None

29. The map method is modified by_____ [ ]

A) Vietch B) charlas C) karnaugh D) none

30. The Sum of product Boolean expression represented the symbol is_____ [ ]

A) π B) ∑ C)€ D)∞

31. The Product of sum Boolean expression represented the symbol is_____ [ ]

A) π B) ∑ C)€ D)∞

32. _____ method is also called as Quine-McCluskey method [ ]

A) K-map B)Tabular C)Graph D)None

33.The minimized expression of Y= A'B'C+A'BC is_____ [ ]

A) A'B B)A'C C)AB D)BC

34. The minimized expression of Y=A'B'C+A'BC+ABC+ABC' is__ [ ]

A) AC+BC B) A+C C)A'C+AB D)AB

35. The Boolean expression is f(A,B,C,D) of m7 representation is [ ]

A) ABCD B) ABC'D' C)A'BCD D)A'B'C'D'

35. The Boolean expression is f(A,B,C,D) of M12 representation is [ ]

A) A+B+C+D B) A+B+C+'D' C)A'+B+C+D D)A'+B'+C+D

36. In K-map using the sequences codes are [ ]

A) Excess-3 B)Gray C)Binary D)BCD

37. 2 NAND gates equivalent to_____ function. [ ]

A)AND 2)OR C)Ex-OR D)Ex-NOR

38. 3 NAND gates equivalent to_____ function. [ ]

A)AND 2)OR C)Ex-OR D)Ex-NOR

39. 2 NOR gates equivalent to_____ function. [ ]

A)AND 2)OR C)Ex-OR D)Ex-NOR

40. 3 NOR gates equivalent to_____ function. [ ]

A)AND 2)OR C)Ex-OR D)Ex-NOR

UNIT – III

Combinational Logic

1. A Combinational circuits consists of _____ [ ]

   A) Input variables B) logic gates C) output variables D) all of these

2. ____ circuits needs two binary inputs and two binary outputs. [ ]

   A) Full adder B) half adder C) sequential D) counter

3. In half adder circuit the inputs are high sum is___ and carry____. [ ]

A) 0,0 B) 0,1 C) 1,0 D) 1,1

4. A ____ is a combinational circuit that converts binary information from n inputs lines to a maximum of 2^n unique output lines. [ ]

A) Encoder B) Decoder C) both A & B D) none of these

5. ____ circuits needs three binary inputs and two binary outputs. [ ]

A) Full adder B) half adder C) combinational logic D) none

6. A decoder with n inputs then itproduce _____ out puts [ ]

A) 2n B) 2^n C)n D) n+2

7. A ____ is a combinational circuit that converts binary information from n inputs lines to a of 2^n unique output lines. [ ]

A) Encoder B) Decoder C) both A & B D) none of these

8. In which circuits memory is not required [ ]

A) Sequential circuits B) synchronous circuits C) both D) none

9. In full adder circuit, the inputs are high sum is___ and carry____. [ ]

B) 0,0 B) 0,1 C) 1,0 D) 1,1

10. In full subtractor circuit, the inputs are high sum is___ and carry____. [ ]

A) 0,0 B) 0,1 C) 1,0 D) 1,1

11. A__is a special combinational circuit designed to compare the binary variables. [ ]

A) Multiplexer B)Decoder C)Comparator D)Demultiplexer

12. A_____ circuit with n inputs and produce 2^n outputs. [ ]

A) Multiplexer B)Decoder C)Comparator D)Demultiplexer

13. _____ circuit acts as inverse operation of a decoder. [ ]

A) Decoder B)Multiplexer C)Encoder D)ALL

14. A _____ circuit with 2^n inputs and produce n data outputs. [ ]

A) Multiplexer B) Encoder C)Decoder D)None

15. In_____, if two or more inputs are equal to 1 at the same time, the input having the highest Priority will take precedence. [ ]

A)Encoder B)priority encoder C)Decoder D)priority encod6er

16. In _____ circuits consists of 2^n inputs with one output [ ]

A) Multiplexer B) Encode C)Decoder D)None

17. In Multiplexer consists of 2^n input lines and ____ selection lines [ ]

A) 2n B) n C) 1 D) 2+n

18. The number of 4*1 multiplexer require to implement 16*1 mux [ ]

A) 5 B) 4 C) 3 D) 8

19. The method of speeding up the process by eliminating inter stage carry delay is called ____ addition [ ]

A) Binary B) Carry Look Ahead C) Parallel D) None

20. Parallel adder is also called as_____ [ ]

A) Binary B) Serial C) Both A&B D) None

21. In half Adder sum simplified expression is [ ]

A) AB+A'B' B) AB'+A'B C) Both A&B D) None

22. Implementation of full adder requires _____ half adders and an _____ gate [ ]

A) 3, AND B) 4, AND C) 2, OR D) 1, OR

23. In parallel adder or subtractor the mode input m=1 the circuit acts as a_____ [ ]

A) Adder B) Subtractor C) Both A&B D) Multiplier

24. In parallel adder or subtractor the mode input m=0 the circuit acts as a_____ [ ]

A) Adder B) Subtractor C) Both A&B D) Multiplier

25. The _____ adder is a sequential circuit [ ]

A) Serial B) parallel C) Both A & B D) None

26. The _____ adder is a Combinational circuit. [ ]

A) Serial B) parallel C) Both A & B D) None

27. The _____ adder is work as slower. [ ]

A) Serial B) parallel C) Both A & B D) None

28. The _____ adder is work as faster. [ ]

A) Serial B) parallel C) Both A & B D) None

29. A_____ is a multiple input and multiple output logic circuits [ ]

A) Multiplexer B) Demultiplexer C) Decoder D) None

30. What are basic gates required to implement a full adder [ ]

A) 1-Ex-OR and 1- AND B) 2-Ex-OR and 1- OR

C) 2-Ex-OR , 2- AND and 1- OR D) 1-Ex-OR , 2- AND and 2- OR

31. In half adder circuit the inputs are 1, 0 then sum is ___ and carry is _____. [ ]

A) 0,0 B) 0,1 C) 1,0 D) 1,1

32. In full subtractor the inputs are low then difference is _____ & barrow is___ [ ]

A) 0,0 B) 0,1 C) 1,0 D) 1,1

33. In full subtractor the inputs are high then difference is _____ & barrow is___ [ ]

A) 0,0 B) 0,1 C) 1,0 D) 1,1

34. Decimal adder is also called as [ ]

A) Binary adder B) BCD Adder C) Binary Subtractor D) None

35. _____ adder uses shift register [ ]

A) Serial B) Parallel C) Both A&B B) None

36. In _____ circuit there are no selection lines [ ]

A) Multiplexer B) Demultiplexer C) Decoder D) None

37. In _____ circuit the selection of specific output line is control by the value of selection lines [ ]

A) Multiplexer B) Demultiplexer C) Decoder D) None

38. In full adder the simplified carry output is [ ]

A) AB+AC+BC B) AB'+A'C+BC' C) A'B+A'C+BC D) None

39. In Half adder the simplified carry output is [ ]

A) BC B) AB C) A'B D) None

40. _____ adder uses register with parallel load capacity [ ]

A) Serial B) Parallel C) Both A&B B) None

UNIT – IV
Synchronous Sequential Logic

1. In D-flip flop the input D=0 the output is _____ [ ]

A) 1 B) 0 C) X D) 10

2. In asynchronous are _____ to design [ ]

A) easy B) difficult C) both A&B D) medium

3. In SR latch the S referred to ____ [ ]

A) Synchronous B) set C) start D) none

4. In T flip flop the input T=1 then Qn+1 is_____ [ ]
   A) Qn B) Qn' C) Qn+1 D) 0
5. In SR latch s=1,r=1 the state is_____ [ ]
   A) No change B) reset C) set D) indeterminate
6. In synchronous counter , if ____ then flip flop complements the input at the time of clock edges [ ]
   A) T=1 B) J=K=1 C) both A & B D) none
7. In Binary counter counts in binary coded decimal from 0000 to ____ and back to 0000.
   A)1001 B) 1111 C) 1000 D) 0000 [ ]
8. 10. In SR latch the R referred to ____ [ ]
   A)Synchronous B) Reset C) set D) none
9. A ____ is a circular shift register with only one flip flop being set at any particular time, all others are cleared. [ ]
   A) ring counter B) shift register C) binary counter D) none of these
10. A sequential circuits consists of _____ [ ]
   A) storage element B) logic gates C) both A& B D) all of these
11. D-flip flop is also known as_____ [ ]
   A) Delay flip flop B) SR latch C) JK flip flop D) none
12. Flip flops are used for_____ [ ]
   A) Memory element B) delay element C) both D) none
13. A J-K flip flop is in " No Change " condition when the value of _____ [ ]
   A) J=0 K=0 B) J=1 K=1 C) J=0 K=1 D) J=1 K=0
14. How is a JK Flip flop made to toggle state [ ]
   A) J=0 K=0 B) J=1 K=1 C) J=0 K=1 D) J=1 K=0
15. In _____ counter all the flip flops are clocked simultaneously [ ]
   A) Asynchronous B)Synchronous C) Ripple D) none of these
16. A J-K flip flop is in " No Change " condition when the value of _____ [ ]
   A) J=0 K=0 B) J=1 K=1 C) J=0 K=1 D) J=1 K=0
17. A ___ is a register for counting the no of clock pulses arriving at its clock inputs. [ ]
   A) Counter B) Register C) Flip Flop D) Decoder
18. How is a JK Flip flop made set state [ ]
   A) J=0 K=0 B) J=1 K=1 C) J=0 K=1 D) J=1 K=0
19. How is a SR Flip flop made set state [ ]
   B) S=0 R=0 B) S=1 R=1 C) S=0 R=1 D) S=1 R=0

20. A ____ is a group of flip flops [ ]
   A) Register B) latches C) counter D) none of these
21. In SR flip flop S=1,R=0 then the state is_____ [ ]
   A) set B) reset C) nochange D) indeterminate state
22. T-flip flop is also known as_____ [ ]
   A) Delay flip flop B) SR latch C) Toggle flip flop D) none
23. In SR latch s=0,r=1 the state is_____ [ ]
   A) No change B) reset C) set D) indeterminate

24. In _____ counter all the flip flops are clocked simultaneously [ ]
A) Asynchronous B)Synchronous C) Ripple D) none of these

25.In SR latch s=1,r=1 the state is_____ [ ]
A) No change B) reset C) set D) indeterminate

26. In which circuits memory is required [ ]
A) Sequential circuits B) synchronous circuits C) bothA&B D) none

27. Examples of sequential circuit_____ [ ]
A) Multiplexer B) Decoder C) flip-flops D) none

28. 64 GB=_____ [ ]
A) 2^{30} B) 2^{36} C) 2^{32} D) none of these

29.In JK flip flop j=1,k=1 then the state is_____ [ ]
A) Q_n^1 B) Q_n C) both D) none of these

30. In which circuits memory is not required [ ]
A) Sequential circuits B) synchronous circuits C) both D) none

31.In synchronous counter , if ____ then flip flop complements the input at the time of clock edges [ ]
A)T=1 B) J=K=1 C) both A & B D) none

32. Master slave flip flop implemented using____ [ ]
A)SR Flip flop B) JK flip flop C) Both A&B D)None

33. In D latch the input is 1 then ouput is ____ state [ ]
A)Synchronous B) set C) start D) none

34. In the binary synchronous counter if the present state of a 4-bit counter is $A_3A_2A_1A_0$=0011, then the next count is _____ [ ]
A) 0010 B) 0100 C) 0101 D) none of these

35. A ____ is a circular shift register with only one flip flop being set at any particular time, all others are cleared. [ ]
A) ring counter B) shift register C) binary counter D) none of these

36. The characteristic equation of SR Flipflop is Qn+1= _____ [ ]
A) S+R'Qn B) S'+RQn C) S+R D) Qn

37. The characteristic equation of JK Flipflop is Qn+1= _____ [ ]
A) JQn'+KQn B) JQn'+K'Qn C) JQn+KQn D) None

38. The characteristic equation of T Flipflop is Qn+1= _____ [ ]
A) TQn'+T'Qn B) TQn'+T'Qn' C) TQn+TQn D) None

39. The characteristic equation of D Flipflop is Qn+1= _____ [ ]
A) DQn B) D'Qn' C) D' D) D

40. _____ sequential circuit is easier to design [ ]
A) Asynchronous B)Synchronous C) Ripple D) none of these

UNIT – V
Memory and Programmable Logic , Digital Logic Circuits

1. RAM performs _____ operations [ ]
   A) Read B) write C) both A&B D)none
2. PAL stands _____ [ ]
   A) Programmable logic array B) programmable array logic C) both A & B D) none
3. A memory write stores binary information in group of bits called_____ [ ]
   A) Words B) bytes C) GB D) none
4. SRAM is made of with _____ [ ]
   A) capacitors B) register C) latches D) counter
5. How many types of memories are used in digital systems? [ ]
   A) 2 B) 3 C) 4 D) 5
6. DRAM abbreviated as _____ [ ]
   A) Delay RAM B)Determinate RAM C)Dynamic RAM D) none
7. To construct 2^k *n ROM is required _____OR gates. [ ]
   A) 2^n B) 2*n C) n+1 D) n
8. When the memory enable input is active, and read/write input value is 1 then which indicates ____ operation to be performed [ ]
   A) read B) write C) both A & B D) none of these
9. In Hamming code method if the data bits are 11 range then the parity bits size is__ [ ]
   A) 5 B) 4 C) 3 D) none of these
10. _____ information is stored in memory [ ]
   A)Binary B) decimal C) octal D) none
11. The process of storing data into the memory is called____ [ ]
   A) read B) write C) delete D) none of these
12. TTL is_____ [ ]
   A) Transistor- Transistor Logic B) Transistor- Transfer Logic
   C) Transistor- Tamsmitter Logic D) none of these

13. The _____ is a programmable logic device with a fixed OR array and a programmable AND array. [ ]
   A) PAL B) PLA C) PROM D) none of these
14. _____ stores the binary information permanently. [ ]
   A) RAM B) ROM C) both A & B D) none of these
15. In Hamming code technique, if the data does not have any error, then C =____ [ ]
   A) 10001 B)0000 C) 1001 D) 1111

16. The _____ is a programmable logic device with a fixed AND array and a programmable OR array. [ ]
   A) PAL B) PLA C) PROM D) none of these
17. A group of eight bits is called a _____ [ ]
   A) Bits B) byte C) kilobyte D) none of these
18. The read only memory is a _____ device [ ]
   A) Programmable logic B) combinational logic C) A & B D) none
19. ROM performs ___operation. [ ]
   A) Read B) Write C) Both A&B D)None

20.Types of ROM memories are_____ [ ]
A) EPROM B) EEPROM C) PROM D) All of these.
21.EEPROM abbreviated as_____ [ ]
A) Erasable – Erasable PROM B) Electrically Erasable PROM
C) Electrically- Electrically PROM D) none of these
22._____ is a nonsaturated digital logic family. [ ]
A) ECL B) TTL C) both A & B D) none of these
23.64 GB=_____ [ ]
A) 2^{30} B) 2^{36} C) 2^{32} D) none of these.

24. The process of transferring the stored data out of memory is referred ___operation.[ ]
A) write B) read C) both A & B D) none
25. The _____ is a programmable logic device with a programmable OR array and a programmable AND array. [ ]
A)PAL B) PLA C) PROM D) none of these.
26. 1 GB=_____ [ ]
A) 2^{30} B) 2^{36} C) 2^{32} D) none of these.
27. _____ is a volatile memory [ ]
A) ROM B) RAM C) PROM D) all
28. RAM is _____memory [ ]
A) Temporary memory B) permanent memory C) both D) none
29.PLA stands _____ [ ]
A)Programmable logic array B) programmable array logic C) both A & B D) none
30.In Hamming code method if the data bits are 7 range then the parity bits size is__ [ ]
A) 5 B) 4 C) 3 D) none of these

31.SRAM abbreviated as _____ [ ]
A) Static RAM B)SetRAM C)Dynamic RAM D) none
32.The process of retrieving data into the memory is called____ [ ]
A) read B) write C) delete D) none of these
33.ECL is_____ [ ]
A) Transistor- Transistor Logic B) Emitter- coupled Logic
C) Emittor- TamsmitterLogic D) none of these
34.A group of 16 bits is called a _____ [ ]
A) Bits B) word C) kilobyte D) 2 words

35.When the memory enable input is active, and read/write input value is 0 then which indicates ____ operation to be performed [ ]
A) read B) write C) both A & B D) none of these
36.A group of 32 bits is called a _____ [ ]
A) Bits B) word C) kilobyte D)Double word
37._____ memory consist of High cost. [ ]

A)SRAM B)DRAM C)Both A& B D)None

38._____ memory consist of low cost. [ ]

A)SRAM B)DRAM C)Both A& B D)None

39.__ erased with an electrical signal instead of ultraviolet light. [ ]

A) Erasable – Erasable PROM B) Electrically Erasable PROM

C) Electrically- Electrically PROM D) none of these

40.placed under a special ultraviolet light for a given period of time will erase the pattern in ROM. [ ]

A)ROM B)PROM C)EPROM D)E^2PROM

Prepared by: **J.Suneetha, Dept.of CSE**